



## DESIGN OF REVERSIBLE THYRISTOR FEED DRIVE WITH PROPORTIONAL-INTEGRAL CONTROLLERS

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**Abstract:** This paper presents a detailed analysis of a reversible thyristor feed drive for industrial metalworking systems, oriented for application in machine tools with position or contour numerical control, as well as in copying and milling machines. The drive under consideration is based on a three-phase zero-reversing scheme, providing a wide dynamic speed control range of the executive motor speed not less than 10000 revolutions, which allows effectively adapting to changes in technological parameters and various production modes. The application of proportional-integral speed and current regulators in the control loop contributes to the accuracy, stability and speed of the system under various mechanical loads and transient modes. The paper offers a comprehensive consideration of structural features, principles of operation and performance characteristics of reversible thyristor feed drive with PI controllers. The obtained results allow to optimize the drive operation in conditions of high precision machining, to expand the functional capabilities of the machine tool equipment, to reduce the influence of external disturbances and to increase the reliability of the industrial system as a whole. The basis of the hardware configuration of the drive consists of thyristor block (BT), control unit (CU), stabilized power supply of control circuits, as well as synchronization transformer, interacting by means of functional blocks: regulator block (RB), phase shifting device (PSD), logic block (BL), stabilized power supply block (SPB) and correction block (BC). The described functional structure simplifies the procedure of initial setting of the drive, tightening the interaction of the system elements and reducing the risk of uneven operation modes. It is possible to use both conventional electric motors with normal inertia-torque ratio and motors with increased torque overload capacity or reduced inertia. An important feature of the proposed solution is a built-in system of protection of power keys against short circuits by using high-speed maximum protection automatics (MPA), which contributes to increased reliability of operation and reduces the risk of failure of expensive elements. Additional stability of thyristor switching process is achieved by using transistor electronic keys, whose operation is synchronized with the supply network due to a special transformer winding, providing fast and accurate transition between positive and negative half-periods.

**Keywords:** *dynamic programming, mathematical model, object control, system behavior.*

### Introduction.

Modern high-precision machine-tool equipment, widely used in a dynamically developing industrial environment, places increased demands on feed and drive systems, which are assigned the functions of precise positioning, contour control and stable operation under the influence of variable loads. In the conditions of tough competition, growing production volumes and rates, as well as the need to optimize operating costs, the development and improvement of power and control systems of

feed drive for numerically controlled machine tools, including positioning and contouring machines, as well as copying and milling systems, is of particular relevance [1].

CNC machines minimize the human factor, ensure the continuity of the production process, increase the accuracy, quality and reproducibility of machining results. To achieve the most efficient operation of such systems is possible only with a harmonious combination of hardware and software components, where a special role is played by feed drives that provide flexible control of speed and position of tools [2]. The use of reversible thyristor feed drives (RTDs) with high dynamic characteristics, an extended speed range, reliable overload protection and the ability to integrate with various types of electric motors opens the way to significant improvements in productivity and the quality of machining complex profiles.

Traditionally, systems with proportional-integral (PI) controllers have been used to control feed drives. Due to their simplicity, stability and predictability, these controllers are widely used in industrial automation. Their use in the thyristor feed drive circuit provides a balance between the accuracy of maintaining the set speed and effective current control, which is especially important for preventing overloads, maintaining stability in transient modes and ensuring long-term trouble-free operation of the equipment [3-6]. Achieving a combination of these goals - stability, accuracy, reliability and a wide control range - is possible through an integrated approach to the design, analysis and experimental debugging of a reversible thyristor drive with PI controllers.

One of the key factors affecting the quality of control is the correct selection and adjustment of the functional units of the actuator. The system under study involves the use of many functional units: regulator unit (RU), phase shifter unit (PSU), logic unit (BL), stabilized power supply unit (SPU) and correction unit (CU). Each of these assemblies contributes to the combined result of optimizing the dynamic and static performance of the actuator. In addition, structurally implemented as a panel with integrated power (thyristor block - BT), control (control unit - CU), as well as additional power supply and synchronization elements, the feed drive can be easily adapted to different operating conditions. The presence of control points in functional blocks simplifies the procedure of initial adjustment, diagnostics and further modernization of the system, providing convenient service and reduced labor intensity of commissioning works.

Another important aspect is to ensure an adequate level of reliability and safety. Under conditions of intensive operation in industrial plants, situations in which there is a risk of short circuits or overloading of power electronics elements inevitably arise. In such cases, the availability of fast-acting maximum protection using high-speed circuit breakers (CBs) becomes critical to prevent the failure of expensive components. The introduction of transistor-controlled electronic keys synchronized to the supply network allows accurate control signals to be generated to the thyristors and increases the overall level of accuracy and consistency of the drive.

Thus, the objective of this study is to present a comprehensive analysis of the design, principles of operation, tuning methodology and performance characteristics of the reversible thyristor feed drive with proportional-integral controllers. The system under consideration is able to provide flexible and reliable speed and torque control, improve the economic performance of production, reduce maintenance costs and increase the stability of the technological process [7]. In the course of the study experimental and theoretical results will be summarized, which allowed to optimize circuit solutions, simplify the procedure of drive integration into existing production lines, as well as to determine the areas of further development and improvement of this class of drive devices.

**Formulation of the problem.**

Modern reversible thyristor feed drives for controlled metalworking systems require an impact, accurate and safe algorithm of control pulse generation. This task is complicated by the fact that in the course of the drive operation it is necessary to provide correct on switching circuit of several logic blocks, phase shifting device (PSD), logic block (BL), regulator block (RB), as well as transistors, capacitors, diodes and pulse transformers, sequences. for generation and transmission of control signals to thyristors. The problem boils down to the strict fulfillment of a set of conditions allowed by the authorities that at any moment of time only pulses are generated that correspond to the active group of thyristors even or odd, ensuring their simultaneous switching on, as well as providing a smooth transition while ensuring the polarity mismatch. In a controlled reversible thyristor drive, there are a number of input signals, hence nodes and conditions on which the actuation and delivery of pulses that open the corresponding thyristors depend. The task is reduced to the following: in the presence of synchronizing signal from synchronizing signal and transformer, control signal (from regulator unit) and at alternation of polarity of supply voltage, to lead sawtooth voltage correctly, to compare it with control signal, to form control pulses of thyristors and to provide impossibility of continuous voltage. switching on of thyristors from even and odd groups [9]. It is necessary to ensure the correct time order of switching on the keys and prevent simultaneous switching on of thyristors from the even and odd group, which will lead to reliable switching and safe direction of inverting.

When the polarity of the mismatch is transmitted (signal at the input of the FSU), the Schmidt trigger returns to the initial state. At this point, the supply of operating pulses of one group is stopped, but the generation of standby pulses for safe inverting continues for a preset time. Logic and external elements protect the absence of overlapping operation modes of thyristor groups and minimize the risk of simultaneous switching on of all keys. To protect the control circuit of thyristors from noise, diode D7 and capacitor C4 are used to stabilize the shape and level of control pulses. The output signal of the FSU has an amplitude of about 6 V at a load current of 0.5 A, beyond the safe opening of thyristors. The functional diagram of the drive is shown in Fig. 1

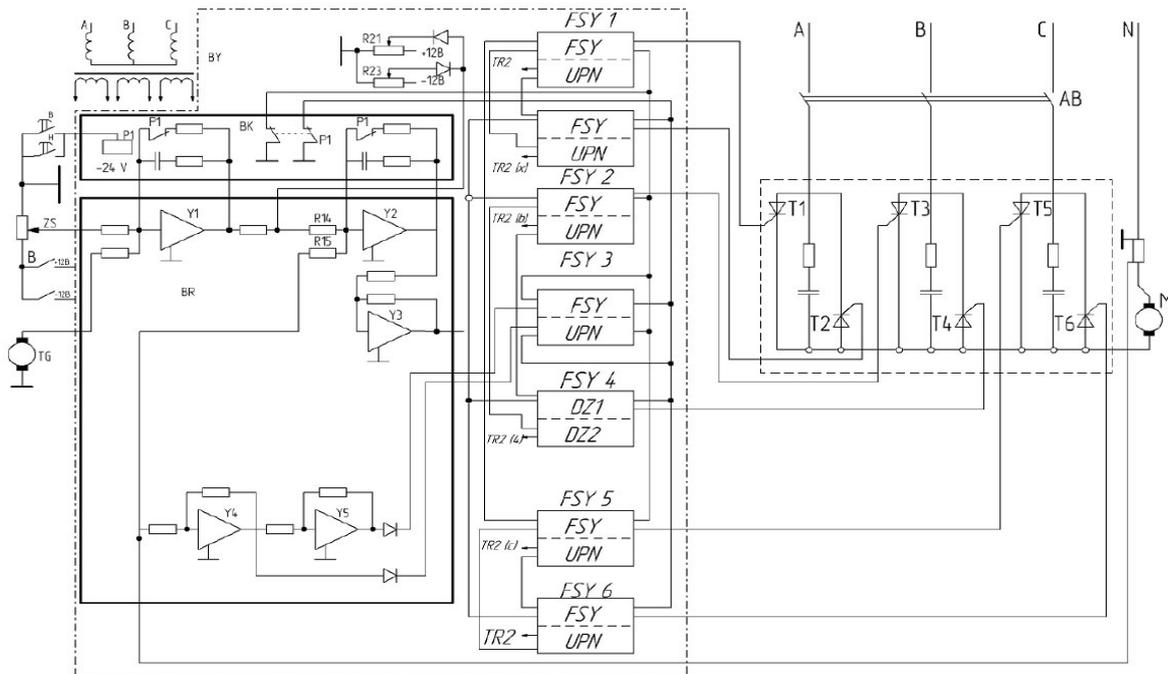


Figure 1. Functional diagram of the actuator

We introduce the following notations and variables:

Synchronization period where  $T$  is the period of the line voltage from which half-periods of duration are reached  $\frac{T}{2}$ .

The voltage is formed on the collector of transistor  $T2$  (through the charge and discharge of capacitor  $C1$  with a slope regulated by potentiometer  $P4$ ).

Its changes vary according to the law

$$Y = f\left(\frac{1}{P4C1}T\right)$$

$f$  - function specifying the line changing in time of increase

The control signal  $Y$  - control coming to the input of the phase shifting device (PSD) from the regulator unit (RU). The control signal coming to the input of the DCS (pin 2) is a command that determines the logic of operation of the PI controllers of pulse frequency and current. The input of this control signal makes it possible to adjust the moment of the Schmidt trigger, thereby changing the phase and time of the control pulses to the thyristors. When the difference between the sawtooth and control signals reaches the trigger threshold, the Schmidt trigger (on transistors  $T4$ ,  $T5$ ) switches from one state to another, generating a rectangular pulse at its output. This rectangular signal is subsequently differentiated using the circuit.  $C3$ ,  $P17$ , generating the sharp negative pulses required to trigger transistors  $T6$ ,  $T7$ . In this way, an accurate timestamp is applied to output the control pulse thyristor.

The power part of the reversible thyristor drive used in numerical or contour program-controlled machine tools is realized by a three-phase zero-phase scheme, which provides the possibility of smooth, symmetrical and reliable reversal of the electric motor rotation. This configuration not only simplifies the transition from one direction of rotation to another, but also contributes to increased stability of operation during load changes. To protect the thyristor keys from emergency conditions such as short circuits in the load or mains faults, a high-speed maximum protection with circuit breaker (CB) is introduced to prevent overheating and failure of expensive semiconductor components. Formation of control signals for thyristors is based on the operation of an electronic key reacting to the voltage coming from the synchronizing winding of the transformer. In the initial phase of each half-period of negative polarity transistor  $T1$  is open, as a result of which capacitor  $C1$  is rapidly discharged through open transistor  $T1$  and diode  $D1$ . This process causes a sharp increase in the positive potential on the collector of transistor  $T2$ , thus forming the initial section of the sawtooth characteristic, which will later be used for comparison with the control signal. In the opposite half-period, when the voltage acquires positive polarity, transistor  $T1$  closes, preventing further discharge of  $C1$ . The capacitor now begins to charge through transistor  $T2$ , resulting in a gradual decrease in the positive potential at its collector. As this potential decreases, the voltage at the base of transistor  $T3$  also decreases, which begins to close smoothly. As a result, a dynamic sawtooth voltage dependence is created in the reference point  $02 U_{02}$ , repeating the trend of voltage change on the collector of  $T2$ . An important aspect of setting up the sawtooth voltage generation unit (VGU) is the possibility of regulating the charge current of capacitor  $C1$ . For this purpose, a potentiometer  $R4$  is included in the base circuit of transistor  $T2$ , which allows changing the sawtooth slope. Thus, by changing the resistance of  $R4$  it is possible to fine-tune the dynamics of sawtooth signal formation,

providing the optimal matching of the time characteristics of the system with the requirements of the technological process.

In addition to the basic function of sawtooth signal generation, the UUT performs the role of a source of duty pulses generated by differentiation of rectangular signals coming from the output of transistor  $T1$ . These duty pulses are fed to contact 11 of the phase shifting device (PSD), operating in counter-phase with this PSD. This signal arrangement optimizes the operation of several DCSs interacting in the same drive system, which is particularly important for reversing or complex operating modes. The phase-shifting device (PSD) has a Schmidt trigger realized on transistors  $T4$  and  $T5$ , a differentiating circuit ( $C3$ ,  $R17$ ), and a power amplifier on transistors  $T6$ ,  $T7$ . In the absence of an input control voltage, transistor  $T4$  is closed and  $T5$  is open, creating the initial steady state of the trigger. Since  $T6$  and  $T7$  are also closed, the output stage of the device is in the ready state without generating control pulses. The resulting sleep mode ensures that parasitic triggering is minimized and protects the thyristors from unnecessary excitation.

The input of transistor  $T4$  receives the sawtooth voltage from transistor  $T3$  and the control signal from the regulator block (RB), which is fed to pin 2 of the FSU. Here the key comparison takes place: when the difference between the sawtooth voltage and the control signal reaches the threshold value, the Schmidt trigger switches over. At this point, a sharp voltage change occurs on the collector of  $T5$  (reference point 03), which corresponds to the formation of a rectangular pulse. The magnitude of the control signal determines the moment at which the trigger switches, thereby setting the phase shift and time reference of the pulses with respect to the line voltage. The rectangular pulses generated by the Schmidt trigger are differentiated using the circuit  $C3$ ,  $R17$ . At its output appear short negative pulses, which serve as “triggers” to turn on transistor  $T6$ , provided there is no prohibition signal from the logic block on pin 6 of the FSU. In parallel, the duty pulses from pin 11, generated by the UUT, are also received here; transistor  $T6$  can be opened either by the operating pulses or by the duty pulses, depending on the current system logic.

In the presence of an enable signal (pin 12 from the logic block), any incoming pulses can turn on transistor  $T6$ , which together with  $T7$  forms a power amplifier. The load of the amplifier is the pulse matching transformer  $T_p1$ . When transistor  $T7$  is triggered, a positive pulse of the specified shape and amplitude (about 6 V at 0.5 A load) is induced in the secondary winding of the transformer. This pulse is fed through diode  $D6$  to the control electrode of the thyristor, and a clear and fast control signal is formed for the power key, which is necessary for stable and predictable control of the drive. Under conditions of polarity mismatch change of the control signal, the Schmidt trigger returns to the initial state ( $T4$  closed,  $T5$  open), which leads to the cessation of operating pulses. At this point, the system does not remain “blind”: the duty pulses continue to flow for a certain time delay set by the logic block to avoid sudden inversion in the absence of clear transients and, therefore, prevents emergencies. To reduce noise in the thyristor control circuit, diode  $D7$  and capacitor  $C4$  are used to stabilize the shape and level of the signal. The logic block ensures that under no circumstances the control impulses to the even and odd groups of thyristors can be supplied simultaneously. Consisting of two identical logic circuits  $LE1$  and  $LE2$ , the logic block ensures that the thyristors of one group can be started only after the thyristors of the other group are completely extinguished. The input of  $LE1$  receives negative pulses from the odd group of FSU, and the input of  $LE2$  receives negative pulses from the even group. These signals form conditions for charging and discharging of capacitors associated with transistors  $T2$  ( $T12$ ), preventing the level required to trigger transistors  $T3$  ( $T13$ ) and  $T4$  ( $T14$ ).

As a result, transistors  $T3$  ( $T13$ ) and  $T4$  ( $T14$ ) remain closed, while  $T5$  ( $T15$ ) remains open and saturated. Closed transistors  $T4$  and  $T14$  provide an enable signal to the corresponding “AND” inputs pin 12 of FSU1, FSU3, FSU5 (for odd-numbered group) or FSU2, FSU4, FSU6 (for even-numbered group). Open transistors  $T5$  ( $T15$ ), included in parallel to the differentiating circuit  $C3$ ,  $R17$  at the input of transistors  $T6$  of the corresponding groups, provide the formation of the prohibition signal, which guarantees a clear separation of logic and excludes the simultaneous appearance of pulses that can cause simultaneous opening of thyristors of even and odd groups. At the moment the odd group of the FSU is operating, and pulses from transistors  $T6$  of this group arrive at the input LE1. Closed transistor  $T4$  of LE1 gives an enable signal to the odd group  $U_{09}$ , If there is a need to switch to the even group, the logic will block the odd group, wait for the complete cessation of its working pulses, and then let the pulses to the even group. This step-by-step switching logic, which relies on negative and standby pulses, ensures safe and reliable reversal of the motor rotation direction, minimizing the risk of equipment damage [10].

The described functionality ensures a high level of reliability and accuracy of the thyristor reversing drive control system. The combination of elements - from the boosters and phase shifters to logic blocks and power amplifiers - forms a coherent mechanism that reacts to changes in input signals and external conditions. This realization allows to accurately dose the moment of thyristors switching on, to prevent the appearance of “conflict” modes of operation and to form stable transients at direction inversion. All this determines high performance, adaptability and safety of the drive operation in the conditions of complex industrial tasks. Since the previously discussed theoretical provisions and structural control schemes of the reversible thyristor drive are much easier to understand when visualized, it is reasonable to proceed to the illustration of these regularities with the help of graphs. The construction of graphical dependencies reflecting the change of the sawtooth signal, control signal and trigger threshold will make it much easier to understand the internal logic of the system operation. For this purpose, below is a sample program code, which, based on the specified parameters, will create a visual graph in the Python environment. xTo analyze the interaction of signals in automatic control systems, a model of a pilot signal accompanied by a control input is often used. This approach provides a clear visualization of signal dynamics and helps identify key threshold values for trigger activation. The presented graph, titled, Fig.2. illustrates the sawtooth pilot signal, control signal, and trigger activation threshold.

```
import numpy as np
import matplotlib.pyplot as plt

# Time parameters
t_end = 0.02 # 20 ms
dt = 1e-5
t = np.arange(0, t_end, dt)

# Parameters for the sawtooth (pilot) signal
f_line = 50
half_period = 1/(2*f_line)
pilot_signal = np.zeros_like(t)
for i, time_val in enumerate(t):
    phi = (time_val % half_period) / half_period
    pilot_signal[i] = phi

# Control signal
U_control_level = 0.5
U_control = np.ones_like(t) * U_control_level

# Trigger threshold
threshold = 0.2
threshold_line = U_control_level + threshold

# Plotting
plt.figure(figsize=(10,5))
plt.plot(t, pilot_signal, label='Sawtooth signal U_pilot', lw=2)
plt.plot(t, U_control, label='Control signal U_control', lw=2)
plt.axhline(threshold_line, color='r', linestyle='--', label='Trigger threshold')
plt.xlabel('Time, s')
plt.ylabel('Voltage, arbitrary units')
plt.title('Sawtooth and control signals with trigger threshold')
plt.legend()
plt.grid(True)
plt.show()
```

*Figure 2. Analysis of pilot and control signals with trigger threshold*

After plotting, we observe the sawtooth signal gradually increases and crosses the period of the control level, and then with the trigger threshold stability when the trigger transitions from one state to another, which leads to accurate parameter selection to achieve stable and inexpensive operation of the driving system, to better understand the prediction.

The chart depicts the voltage versus time for both a sawtooth signal  $U_{pilot}$  and a control signal  $U_{pilot}$ . The red line corresponds to the sawtooth signal  $U_{pilot}$ , which exhibits alternating positive and negative peaks. In contrast, the blue line represents the control signal  $U_{control}$ , which remains relatively constant throughout the measurement period. The horizontal axis is labeled as "Time, s," indicating the time interval, while the vertical axis is marked as "Voltage, arbitrary units," showing the magnitude of the voltage Fig. 3.

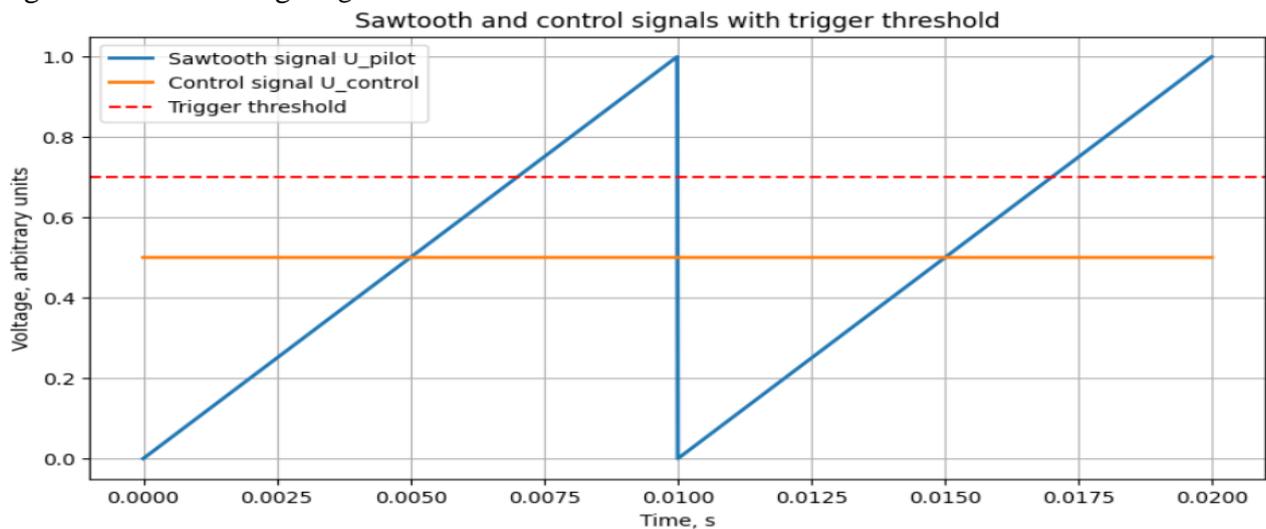


Figure 3. Sawtooth and control signals with trigger threshold

The abscissa axis specifies the time in seconds, e.g. from 0 to 0.02 s (20 ms). The start point is 0 s and the end point is 0.02 s. The time step is so small that the curve looks smooth and continuous. In the graph there is a curve going from points (0, 0) in low voltage mode to point (0.01, 1), that is, for half of the period (about 10 ms) the voltage line increases from 0 to 1. Then, starting at 10 ms, the signal drops back to 0 as the sawtooth signal repeats every half-periodic portion of time. The graph looks like the “teeth of a sawtooth”: it angles upward, reaches a maximum (1), and then abruptly zeroes out to 0, forming this rising line. If we consider only one half-period - it is just a line growing from left to right.

Since we are only looking at 20 ms (and at 50 Hz the half-period is ~10 ms), we see two saw teeth:

1. From 0 to 10 ms: the line rises smoothly from 0 to 1.
2. At around 10 ms, the signal returns to 0 again.
3. From 10 to 20 ms it grows from 0 to 1 again.

On the same chart there is a horizontal straight line at the level of 0.5 on the ordinate axis, a vertical axis, a flat line (without slope) is drawn along the entire time interval, at half height of the chart, dividing the visual chart field approximately in half vertically.

Another horizontal dashed or indicating line, for example the color red, is drawn at the level of 0.7 is  $0.5 \pm 0.2$ , where 0.5 is the level of the control signal, and 0.2 is the threshold. What is above the control signal line. It remains at 0.7 continuously throughout the time interval.

- X-axis: time from 0 to 0.02 s.

- Y-axis: voltage from 0 to just above 1 (to move the 0.7 threshold line and sawtooth signal to 1).
- At the bottom of the graph is a toothy rising signal (sawtooth) that goes from 0 to 1 in 10 ms.
- Just below the height is the control line  $U_{control} = 0.5$ .
- Even higher is the dotted line of the trigger threshold at 0.7.

Between 0 and 10 ms the sawtooth signal (the line going up horizontally) crosses the control signal level (0.5) at about dawn, the threshold line 0.7 a little later, we can see the sawtooth rising and at a certain point the threshold turns, which corresponds to the trigger time.

As a result, there are three main elements in one graph: the rising sawtooth signal, the horizontal line of the control signal and the horizontal line of the threshold we can see the relationship between the sawtooth voltage waveform, the level of the control signal and the trigger threshold.

### **Solution of the problem**

To ensure stable, accurate and safe operation of reversible thyristor feed drive with regard to the inclusion of “creeping” speed, to preserve the output voltage in the stable power supply unit (SPU), as well as to prevent unauthorized inclusion of thyristors in the same group at a signal at the input, a complex system is proposed. It is based on the generator frequency regulator, current, inverter, logic elements and stabilized power supply unit.

At normal closing of the contacts of the interlock relay R1 is shunted feedback circuits of amplifiers U1 and U2, as well as the outputs of logic elements LE1 and LE2. Due to this, even minimal control signals in the actuator are blocked in the absence of applied setpoint voltage, e.g. when direction relays “B” or “H” are not switched on. This measure ensures that the actuator does not tend to accelerate to a creeping speed without additional operator or control program assignment.

Formally, we can represent the state of the creeping velocity state through the system.

Let

$$Y(m) = 0, \forall m \notin [m_0, m_1],$$

where  $Y(m)$  - setpoint voltage at the drive input. The interlocking is then ensured:

$$Y(m) \approx 0, \forall m \notin [m_0, m_1],$$

detection of the occurrence of non-zero output torque or speed.

The stabilized power supply employs two identical stabilizers that function by using compound transistors (e.g., T8, T2) as a variable resistor. This approach keeps the output voltage constant, regardless of load or input voltage fluctuations. The reference circuitry within the regulator analyzes the difference between the reference voltage (generated by stabilizer D6) and the actual output voltage taken from dividers R7, R8, R9.

Let

$$Y = const$$

is set by stabilizer D6. Output voltage of the stabilizer:

$$Y = Y \frac{P_8 + P_9}{P_8}$$

provided that the resistances R7, R8, R9 are selected accordingly. If for some reason  $Y_{max}$  of the set level, it increases the voltage across the divider, consequently, the input signal on the base of transistor T3 increases:

$$Y_{base}(T3) = F(Y) > Y_{base}$$

This leads to an increase in its collector current:

$$R_C(T3) = K_{T3}(Y_{base}(T3) - Y_{base})$$

where  $K_{T3}$  is the gain of transistor T3.

The rising current of T3 partially locks the composite transistor T8, T2, increasing its differential resistance P

$$P_{T8,T2}(m) = P_{T8,T2}^{\min} + \Delta R(R_C(T3)),$$

which leads to voltage drop on T8, T2 and restoration of equilibrium:

$$Y(m) \rightarrow Y = const$$

In this way, the system automatically restores the output voltage to the specified customer in case of any disturbance.

The current level limits in the drive are set by potentiometers R21, R23, the possibility of switching between different potentiometers with the machine node selection switch provides flexible adaptation of the drive under the motor of different power. Formally it can be described as follows:

Let  $\Delta UC$  be the control voltage increment for current limitation,  $\alpha p$  be the adjustment factor of the potentiometer. Then:

$$R_{lim} = R \left( \frac{Y \pm \Delta U_c}{Y} \right) \alpha p$$

where  $R_{lim}$  - level of the new current limitation after adjustment with the potentiometer.

By selecting the switching relay, it is possible to change  $\alpha p$ , adjusting to a different motor power, thus saving time and simplifying the integration of different units.

The amplifier block ( $Y1$  - frequency controller,  $Y2$  - current controller,  $Y3$  - inverter,  $Y4$  - current amplifier,  $Y5$  - current inverter) at least integral amplifiers with a transfer coefficient  $10^5$  large input impedances ( $\geq 10^5 \Omega$ ) are used, which allows minimizing losses and restoring the signal. The low temperature drift of no more than  $10mcV / C^\circ$  ensures the stability of the system operation in various temperature regimes. Conditional balanced mode for one of the amplifiers under consideration:

$$Y = A \cdot (Y_v^+ - Y_v^-)$$

where

$A$  - coefficient transfer,  $Y_v^+$ ,  $Y_v^-$  - input signals.

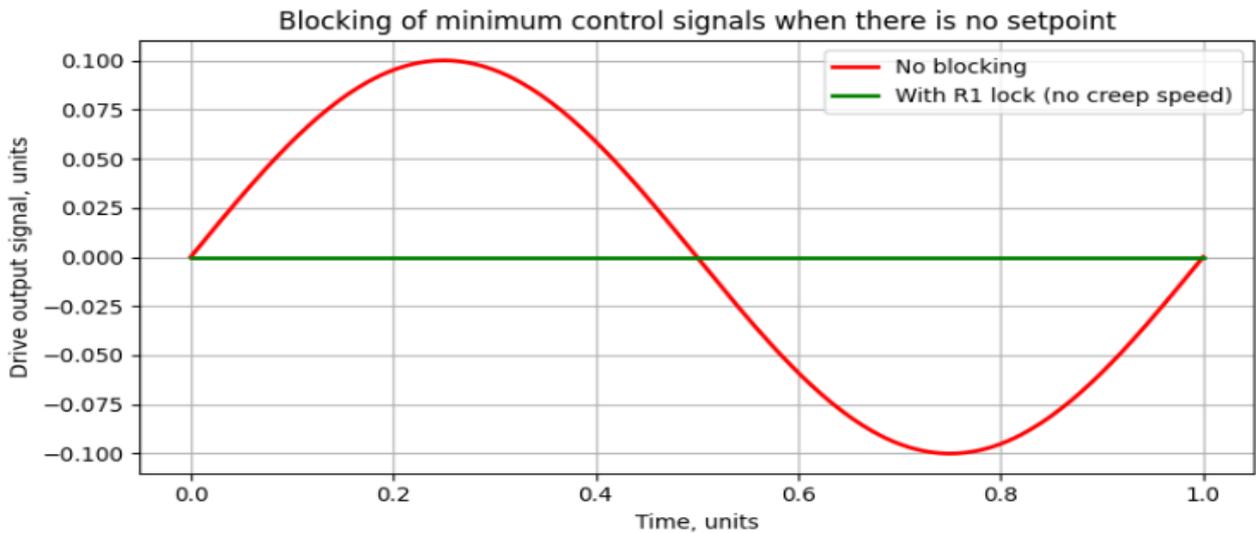
At  $A \rightarrow 10^5$ , even a small difference between the inputs results in a significant output signal, which improves the control accuracy. The temperature drift  $\Delta U$  can be estimated as follows:

$$\Delta U \approx 10mcV / C^\circ$$

which, under the right operating conditions, is very small.

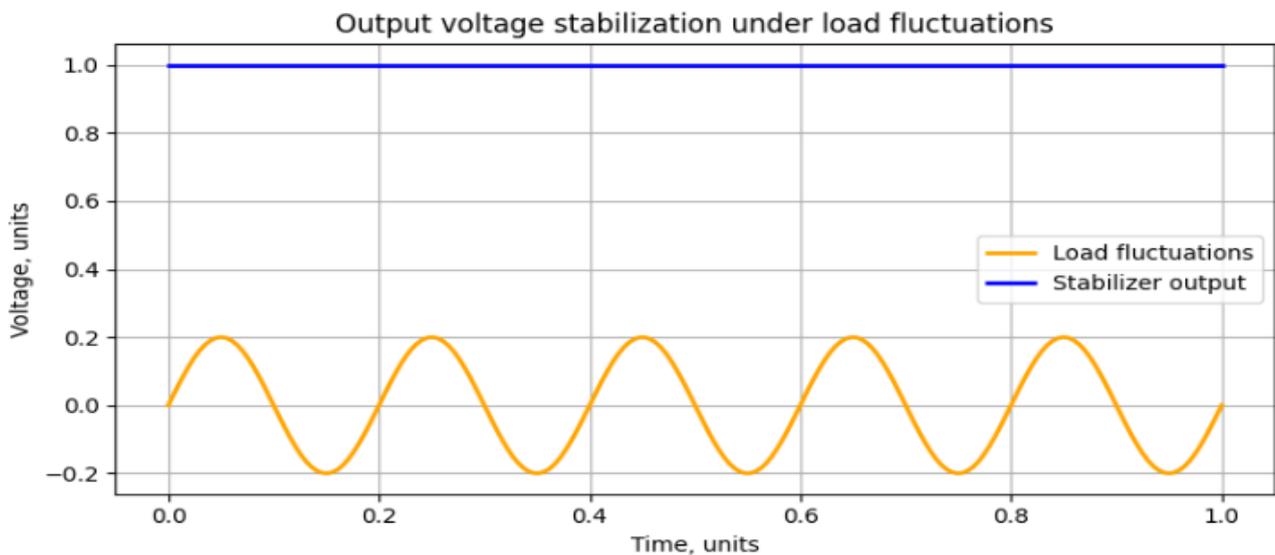
Let's move on to plotting the graphs to illustrate how these processes and settings are reflected over time or when parameters are changed.

The graph below depicts Fig.4 the blocking of minimum control signals when there is no setpoint. It shows the relationship between signal output and time for two different conditions: without blocking and with  $R1$  lock no creep speed. This is a crucial tool for analyzing safety system performance, helping to understand how various parameters affect device operation in real-world scenarios.



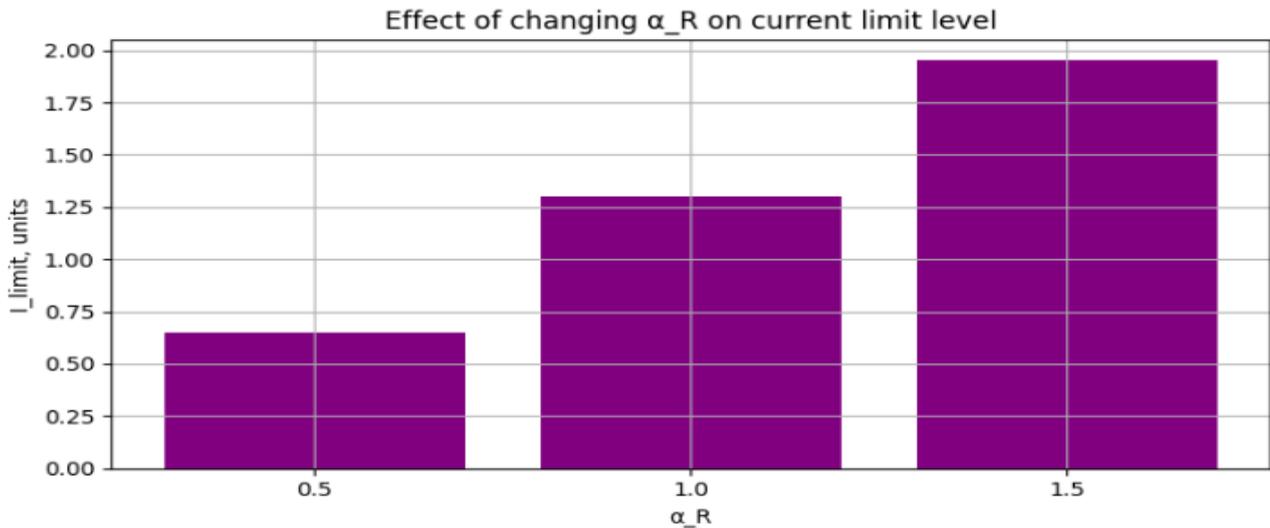
*Figure 4. Blocking the «creeping» speed*

This graph demonstrates the difference between the operation of the actuator with interlocking. In the absence of setpoint voltage, normal operation of the interlock relay R1 ensures that there are no even minimal control signals - the output signal remains at zero. Without interlocking, small oscillations can be seen, which could cause the mechanism to "creep". This comparison clearly shows the effectiveness of interlocking in preventing unwanted actuator movement in the absence of a command. On the previous slide, we examined the theoretical foundations of voltage stabilization under load conditions, including the impact of various factors such as signal frequency and amplitude. Now let's move on to a practical example shown in Fig.5.



*Figure 5. Output voltage stabilization*

Here we see the behaviour of the stabiliser despite load fluctuations, the output voltage remains constant, the stabiliser successfully smooths out any fluctuations, ensuring stable operation of the drive units and control electronics, regardless of changing output conditions. Now let's move on to the practical application of these concepts using this graph. This graph shows the effect of changing parameter  $\alpha_r$  at the current limit level Fig.6.



*Figure 6. Flexibility of setting the current limit via  $\alpha_R$*

Changing the coefficient  $\alpha_R$  affects the level of current limitation. A higher  $\alpha_R$  increases the maximum permissible current and a lower  $\alpha_R$  reduces it, as it allows the drive to be adapted to different motors varying in power and requirements by simply switching potentiometers and selection relays.

All amplifiers are fitted with oscillating circuits. Zero balancing circuits are provided in amplifiers U1, U4.

The correction circuits of amplifiers U1 and U2 are located in the correction block (BC). The level of current limitation is set by potentiometers R21, R23, installed outside the block, and is determined by the formula:

$$I_{T0} = \frac{1}{K_T} \times \frac{R15}{R14} U_{y1}$$

where  $I_{T0}$  is the level of current limitation;

$K_T$  - current feedback coefficient equal to the shunt transfer coefficient  $1.5 \cdot 10^{-3} V \cdot A$  - for 50 A shunt, 75 mV;

$U_{y1}$  is the maximum output voltage of the amplifier U1, coming to the input of U2, i.e. the voltage determined by resistors R21, R23.

Let's try to map the X-axis in time for several signals:

Enable signal for the odd group of DCFs, up to the moment  $t_1$  the group is active, then when the sign of the control voltage on the side of U3 changes, the access is switched off after a pause  $\Delta t_1$ . Enable signal for even-numbered group of DCFs: it is enabled only after an additional pause  $\Delta t_2$ , ensuring a smooth transition. Armature current  $I_y$ , during odd group operation the current is maintained at a certain level, then when the operating pulses are stopped and only duty pulses are applied during  $\Delta t_2$  the current drops rapidly to zero. Events in time, where moment  $t_1$  - change of sign of voltage U3, beginning of pauses, moments of removing and setting permissions.

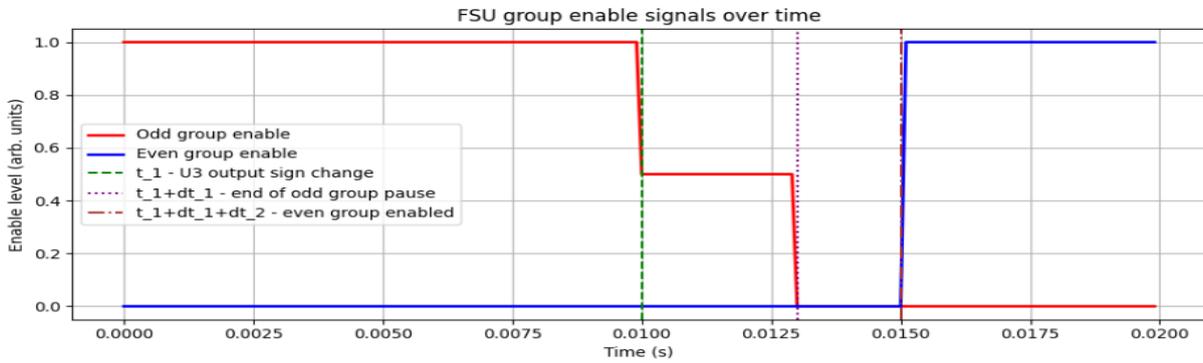
Let's say:

- $t_1 = 0.01$  s - change of sign of voltage at the output of U3.
- $\Delta t_1 = 0.003$  s - pause during which the current decreases.

- $\Delta t_2 = 0.002$  s - pause before switching on the even group after  $\Delta t_1$ .

In load distribution control systems, particular attention is paid to the algorithms responsible for enabling and disabling different groups of components. These algorithms ensure balanced load distribution and minimize delays during switching operations. The graph below provides a detailed depiction of the timing of activation signals for the odd and even groups labeled as odd group and Even group during the control process. Key moments are highlighted on the graph, such as the sign change of the output signal  $U_3$  denoted as  $t_1$ , the end of the pause for the odd group  $t_1 + dt_1$ , and the activation of the even group  $t_1 + dt_1 + dt_2$ . These events are visually distinguished using color-coded markers to simplify identification and analysis.

This visualization helps evaluate the efficiency of switching between groups and identify potential areas for optimization, such as minimizing pause durations or improving synchronization. Let us now examine the graph titled Fig. 7 for a more detailed analysis of the system's behavior.

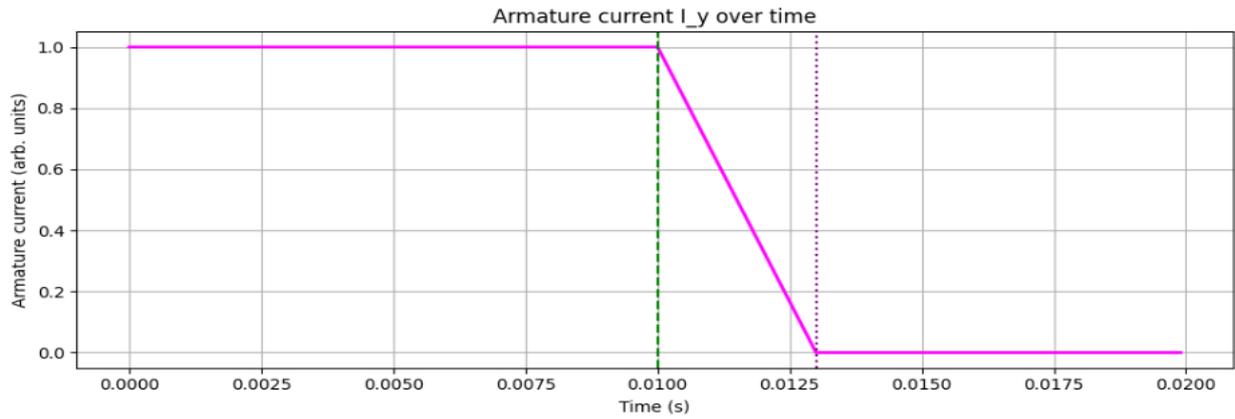


*Figure 7. FSU group enable signals over time*

At time  $t_1$ , when the sign of the voltage at the output of  $U_3$  changes, the resolution for the odd group is gradually removed. At first, only duty pulses are applied during  $\Delta t_1$ , then the permission disappears completely. Only after an additional pause of  $\Delta t_2$  does the resolution change to the even group. This visual representation underlines the organised sequence of actions aimed at preventing the impulses of the two thyristor groups from overlapping and guaranteeing safe switching.

The behavior of the armature current  $I_y$  over time plays a crucial role in understanding the dynamics of the load distribution system. This parameter is directly influenced by the enabling signals of the odd and even groups, as well as the timing of the system's switching operations. By analyzing the graph, we can observe how  $I_y$  responds to these control actions, providing insights into system performance and stability.

The graph titled Fig. 8 armature current  $I_y$  over time illustrates the temporal evolution of the current. Key moments are marked for clarity, including the signal sign change  $t_1$  and the end of the odd group's pause  $t_1 + dt_1$ . These points signify critical transitions in the control process, directly impacting  $I_y$ . The visual representation highlights the decrease in armature current after  $t_1$ , reflecting the system's response to the control algorithm. This data is vital for assessing how efficiently the system handles load transitions and identifying potential improvements in current regulation mechanisms.

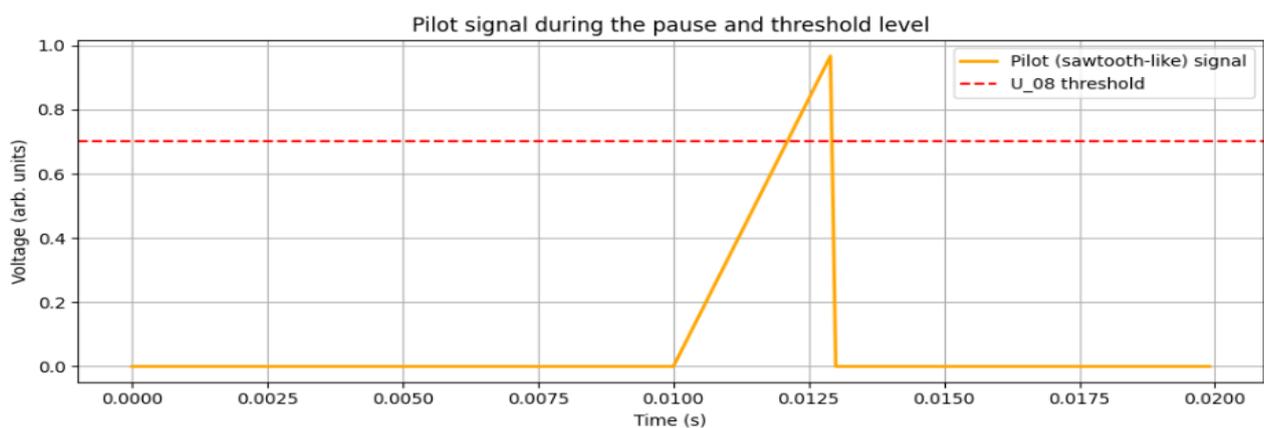


*Figure 8. Armature current  $I_y$  over time*

The armature current  $I_y$  is maintained at a stable level until  $t_1$ . At the moment  $t_1$ , the current is rapidly discharged by means of duty pulses only. During the time  $\Delta t_1$ , the current drops rapidly to zero, which prevents dangerous transients and guarantees a soft termination of one of the groups.

The dynamics of the pilot signal are instrumental in regulating the system during critical operational phases, such as pauses and threshold evaluations. The graph titled Fig. 9 pilot signal during the pause and threshold level, provides a detailed view of the voltage variations of the pilot signal sawtooth-like in comparison to the threshold  $U_{08}$ .

This representation shows the behavior of the pilot signal, characterized by its sawtooth waveform, alongside the fixed threshold level, marked as a red dashed line. Notably, the intersection between the pilot signal and the threshold signifies critical triggering points, essential for initiating specific control actions within the system. From the graph, we observe the periodic nature of the pilot signal and its ability to reset upon reaching the threshold, which ensures synchronization and stability in the control process. Analyzing these interactions helps evaluate the system's responsiveness and the effectiveness of the set threshold in maintaining desired operational conditions. This graphical insight lays the foundation for optimizing signal configurations and refining system control strategies.



*Figure 9. Pilot signal during the pause and threshold level*

Limiting the maximum level of the control voltage applied to the phase-shifting devices (PSDs) is carried out by stabiliser D2, which ensures that the amplitude of the input signal does not exceed the maximum permissible values.

If the system is used in a single motor configuration, a standard jumper is connected between pins 16-17 of connector III2 on the external side. If the drive serves several motors with different

power characteristics, external current limiting potentiometers are connected to pins 16-17 via the machine unit selection relay. The important prerequisite is the sequence of operation. The voltage sawtooth device (VDU) and the associated phase-shifting device are placed on a single printed circuit board, ensuring compactness and reducing noise sensitivity. The VVM consists of an electronic key on transistor T1, a current stabiliser on transistor T2 and an emitter repeater on transistor T3. The sawtooth signal is formed during the charging of capacitor C1, and the charging current is set by the base bias determined by the ratio of resistances R3 and R4. A stable sawtooth slope required for accurate phase p is provided.

The circuits of logic elements provide modes of mutual blocking and delay of permissive signals. Thus, open transistor T5 of the LE1 circuit shunts the input of transistor T6 of the even group of FSU, and also short-circuits the LE2 input on terminals 18-20, forming the prohibition signal  $U_{04}$  for the even group of FSU. Suppose that at time  $t_1$  at the output of the amplifier U3 of the regulator block, BR changes the sign of the voltage, as a result of which the working impulses from the odd-numbered group of DCF cease to arrive at the input LE1. As a result, transistor T2 of the LE1 circuit closes, and capacitor C1 during the pause  $\Delta t_1$  is charged to the triggering voltage of transistor T3  $U_{08}$ . The pause  $\Delta t_1$  is determined by the time constant of the circuit R4C1, as well as by the level of the signal proportional to the armature current coming from the output of the inverter of the current amplifier U5 of the BR unit. During this time interval  $\Delta t_1$ , only duty pulses are supplied to the thyristors of the odd group, accelerating the armature current reduction to an acceptable low level. After the pause  $\Delta t_1$ , transistor T4 opens, removing the permission from the odd group of DCFs, and the duty pulses are no longer supplied to the corresponding thyristors. C  $\Delta t_2$ , determined by the time constant of the C2R8 circuit. This time delay  $\Delta t_2$  is critical to guarantee that the current in the previously operating group is reduced to zero.

At the end of the pause  $\Delta t_2$ , the logic circuit LE2 transfers control to the even group of DCFs. The operating pulses of this group start to flow from transistors T5 of the even branch to the input of LE2, forming the signal  $U_{04}$ . When the first pulse in LE2 discharges capacitor C11, and without any additional delay, the prohibition signal is fed to the odd group of DCF, because the transistor T15, opening, shunts the input of transistors T6 of the odd group.

The closing of transistor T14 at this moment gives an enable signal for the even group of DCFs. The operating and standby pulses are fed back to the thyristors of the even group, ensuring a smooth and safe control transition as well as synchronisation of the drive operating modes during reversing or changing load conditions.

### **Results and conclusions.**

The use of specialised correction blocks, potentiometers for setting current limiting levels and machine node selection relays makes the drive extremely flexible. The use of proportional-integral controllers, amplifiers with high gain of the order of  $10^5$ . makes it possible to achieve stable and accurate maintenance of the set parameters. This results in stabilisation of the speed of rotation, accurate holding of the allowable current and maintenance of the required accuracy in the control loop even under significant changes in load or external conditions. The inclusion of an interlock relay and logic element circuit, as well as the correct organisation of the operating and standby pulses applied to the thyristors of both groups of DCFs, ensures that the drive will not spontaneously reach minimum speed in the absence of a setpoint signal. Implementation in the stabilised power supply

unit of comparison circuits with reference stabilatron and use of compound transistors as variable resistance ensures constant level of output voltage in case of load fluctuations or changes in input parameters.

The logic of delays ( $\Delta t_1$ ,  $\Delta t_2$ ), duty and working pulses, as well as the sawtooth voltage control ensures a smooth transition between odd and even groups of DCFs during reversing. Transients are controlled predictably, armature current has time to decrease to a safe level, after which another group is connected without the risk of overlapping or simultaneous switching on of thyristors of different branches. This approach minimises the risk of damage, overheating and unwanted mechanical shocks in the drive. Low temperature drift of integrated amplifiers, optimal selection of resistors, stabilisers and transistors in stabilisation and correction circuits allow to guarantee stability of control parameters in a wide range of temperatures and external conditions. As a result, the reliability and durability of the drive is increased, and the need for frequent adjustments and readjustments is reduced. All these aspects form a complete, integrated control system for reversible thyristor drive, characterised by high accuracy, safety, adaptability and stability

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